IN THE CLAIMS

Please amend the claims as indicated below.

1. (canceled)

2. (canceled)

3. (previously presented) A method for making a semiconductor device, comprising:

providing a substrate with an upper surface, the substrate having a trench therein;

providing an oxide layer on a bottom and sidewall of the trench;

providing a conductive layer on a bottom and sidewall of the oxide layer, the conductive layer having an upper surface below the upper surface of the substrate; and

providing a self-aligned isolation cap on the conductive layer within the trench, the isolation cap comprising a non-organic dielectric material, including providing the self-aligned isolation cap by providing a first dielectric layer, providing a second dielectric layer over the first dielectric layer, reflowing the second dielectric layer, and then anisotropically etching the first and second dielectric layers until the upper substrate surface is exposed.

4. (previously presented) The method of claim 3, including reflowing the second dielectric layer until an upper surface of the second dielectric layer is substantially planar.

5. (currently amended) The method of claim 3 ~~claim 1~~, wherein the conductive layer comprises polysilicon or metal.

6. (previously presented) A method for making a semiconductor device, comprising:

providing a semiconductor substrate with an upper surface, the substrate having a trench therein;

providing a gate oxide layer on a bottom and sidewall of the trench;

providing a conductive layer on a bottom and sidewall of the oxide layer, the conductive layer having an upper surface below the upper surface of the substrate; and

providing a self-aligned isolation cap on the conductive layer and only within the trench by using a combination of dielectric materials with different etching rates.

7. (previously presented) A method for making a semiconductor device, comprising:

providing a substrate with an upper surface, the substrate having a trench therein;

providing an oxide layer on a bottom and sidewall of the trench;

providing a conductive layer on a bottom and sidewall of the oxide layer, the conductive layer having an upper surface below the upper surface of the substrate; and

providing a self-aligned isolation cap on the conductive layer within the trench by using a combination of dielectric materials with different etching rates, including providing the self-aligned isolation cap by providing a first dielectric layer having a first etching rate in the trench and on the upper substrate surface, providing a second dielectric layer having an etching rate faster than the first etching rate on the first dielectric layer, reflowing the first and second dielectric layers, and then isotropically etching until the upper substrate surface is exposed.

8. (original) The method of claim 7, including reflowing the first and second dielectric layers until the upper surface of the second dielectric layer is substantially planar.

9. (original) The method of claim 7, wherein the first dielectric layer dielectric material comprises PSG, BPSG, or a low-temperature oxide.

10. (original) The method of claim 7, wherein the second dielectric layer dielectric material comprises PSG or BPSG.

11. (original) The method of claim 7, wherein the conductive layer comprises polysilicon or metal.

12. (previously presented) A method for making a semiconductor device, comprising:

providing a semiconductor substrate with an upper surface;

providing a nitride-containing layer on a first portion of the substrate upper surface;

providing a trench in a second portion of the substrate, the second portion not containing the nitride-containing layer thereon;

providing a gate oxide layer on a bottom and sidewall of the trench;

providing a conductive layer on a bottom and sidewall of the oxide layer, the conductive layer having an upper surface below the upper surface of the substrate;

providing a self-aligned isolation cap on the conductive layer within the trench; and

removing the nitride-containing layer.

13. (previously presented) The method of claim 12, wherein the upper surface of the conductive layer and the substrate upper surface are separated by about 0.5 microns.

14. (previously presented) The method of claim 12, the conductive layer comprising polysilicon.

15. (previously presented) The method of claim 14, including providing the self-aligned isolation cap by oxidizing the upper surface of the conductive polysilicon layer.

16. (previously presented) The method of claim 12, including providing the self-aligned isolation cap by selectively depositing a dielectric layer on the upper surface of the conductive layer.

17. (original) The method of claim 12, wherein the conductive layer comprises polysilicon or metal.

18. (canceled)

19. (canceled)

20. (canceled)

21. (canceled)

22. (previously presented) A method for making a MOSFET, comprising:

providing a semiconductor substrate with an upper surface, the substrate having a trench therein;

providing source and channel regions proximate the trench;

providing a gate oxide on a bottom and sidewall of the trench;

providing a conductive gate on a bottom and sidewall of the gate oxide, the conductive gate having an upper surface below the upper surface of the substrate; and

providing a self-aligned isolation cap on the conductive gate within the trench by using a combination of dielectric materials with different etching rates.

23. (previously presented) A method for making a MOSFET, comprising:

providing a substrate with an upper surface, the substrate having a trench therein;

providing source and channel regions proximate the trench;

providing a gate oxide on a bottom and sidewall of the trench;

providing a conductive gate on a bottom and sidewall of the gate oxide, the conductive gate having an upper surface below the upper surface of the substrate; and

providing a self-aligned isolation cap on the conductive gate within the trench by using a combination of dielectric materials with different etching rates, including providing the self-aligned isolation cap by providing a first dielectric layer having a first etching rate in the trench and on the upper substrate surface, providing a second dielectric layer having an etching rate

faster than the first etching rate on the first dielectric layer, reflowing the first and second dielectric layers, and then isotropically etching until the upper substrate surface is exposed.

24. (previously presented) A method for making a MOSFET, comprising:

providing a semiconductor substrate with an upper surface;

providing source and channel regions in the substrate;

providing a nitride-containing layer on a first portion of the substrate upper surface;

providing a trench in a second portion of the substrate, the second portion not containing the nitride-containing layer thereon;

providing a gate oxide on a bottom and sidewall of the trench;

providing a conductive gate on a bottom and sidewall of the gate oxide, the conductive gate having an upper surface below the upper surface of the substrate;

providing a self-aligned isolation cap on the conductive gate within the trench; and

removing the nitride-containing layer.

25. (canceled)

26. (canceled)

27. (canceled)

28. (canceled)

29. (canceled)

30. (canceled)

31. (canceled)

32. (new) The method of claim 3, wherein the self-aligned isolation cap comprises silicon oxide.

33. (new) The method of claim 3, wherein the first dielectric material comprises PSG and the second dielectric material comprises BPSG.

34. (new) The method of claim 6, wherein the dielectric materials comprises PSG, BPSG, or a low-temperature oxide.

35. (new) The method of claim 6, wherein the different etching rates are provided by doping one or both of the dielectric materials.

36. (new) The method of claim 34, wherein one of the dielectric materials comprises PSG and another dielectric material comprises BPSG.

37. (new) The method of claim 6, wherein the conductive layer comprises polysilicon or metal.